// Half Adder in Verilog

module half\_adder (

input wire a, b, // Inputs

output wire sum, // Sum output

output wire carry // Carry output

);

// Logic equations

assign sum = a ^ b; // XOR for sum

assign carry = a & b; // AND for carry

endmodule

// Full Adder in Verilog

module full\_adder (

input wire a, b, cin, // Inputs

output wire sum, carry // Outputs

);

// Logic equations

assign sum = a ^ b ^ cin; // XOR for sum

assign carry = (a & b) | (b & cin) | (a & cin); // Majority function for carry

endmodule

// Half Subtractor in Verilog

module half\_subtractor (

input wire a, b, // Inputs

output wire diff, borrow // Outputs

);

// Logic equations

assign diff = a ^ b; // XOR for difference

assign borrow = ~a & b; // Borrow when a < b

endmodule

// Full Subtractor in Verilog

module full\_subtractor (

input wire a, b, bin, // Inputs

output wire diff, borrow // Outputs

);

// Logic equations

assign diff = a ^ b ^ bin; // Difference

assign borrow = (~a & b) | (~(a ^ b) & bin); // Borrow logic

endmodule